Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

1 (currently amended). ~~A~~ An integrated circuit including a top metal level capacitor ~~for integrated circuits~~, comprising:

a plurality of levels of metal conductors disposed near a surface of a semiconductor substrate, the plurality of levels including a top metal level that is disposed furthest from the surface of the plurality of levels;

a bottom electrode, said bottom electrode positioned over a the top metal level and ~~coupled to~~ conductively contacting a first ~~interconnect~~ conductor of said top metal level;

a capacitor dielectric ~~coupled to~~ disposed over said bottom electrode;

~~a top electrode coupled to said capacitor dielectric; and~~

~~sidewalls positioned at a perimeter of said top metal level capacitor; said sidewalls coupled~~ dielectric sidewall structures disposed adjacent to ~~said top metal level,~~ said bottom electrode, and at least a portion of said capacitor dielectric; and ~~, and a portion of said top electrode; wherein said top electrode is coupled to a second interconnect of said top metal level~~

a top electrode, disposed over said capacitor dielectric and extending over at least one dielectric sidewall structure to conductively contact a second conductor of said top metal level.

2 (currently amended). The integrated circuit ~~top metal level capacitor~~ of Claim 1 wherein the capacitor dielectric is comprised of a high-k material.

3 (currently amended). The integrated circuit ~~top metal level capacitor~~ of Claim 2 wherein said capacitor dielectric is TaO_x.

4 (currently amended). The integrated circuit ~~top metal level capacitor~~ of Claim 1 wherein said bottom electrode is comprised of a layer of TaN and a layer of TiN.

5 (currently amended). The integrated circuit ~~top metal level capacitor~~ of Claim 1 wherein said top electrode is comprised of a layer of TiN and a layer of TaN.

6 (currently amended). The integrated circuit ~~top metal level capacitor~~ of Claim 1 wherein said ~~sidewalls~~ dielectric sidewall structures are comprised of SiN.

7 (currently amended). The integrated circuit ~~top metal level capacitor~~ of Claim 1 wherein said ~~first interconnect and said second interconnect~~ conductors in said top metal level are comprised of Cu.

8 (currently amended). The integrated circuit ~~top metal level capacitor~~ of Claim 1 wherein said first ~~interconnect~~ conductor is coupled to a power supply rail.

9 (currently amended). The integrated circuit ~~top metal level capacitor~~ of Claim 1 wherein said second ~~interconnect~~ conductor is coupled to ~~GND~~ ground.

10 (currently amended). The integrated circuit ~~top metal level capacitor~~ of Claim 1 wherein said top metal level capacitor is a decoupling capacitor from a supply voltage to ground.

11 (currently amended). ~~A~~ An integrated circuit including a top metal level capacitor ~~for integrated circuits,~~ comprising:

a plurality of levels of metal conductors disposed near a surface of a semiconductor substrate, the plurality of levels including a top metal level comprised of copper that is disposed furthest from the surface of the plurality of levels;

a bottom electrode comprised of a layer of TaN and a layer of TiN, said bottom electrode positioned over ~~a top metal level and coupled to~~ and in contact with a first ~~interconnect~~ conductor of said top metal level;

a capacitor dielectric comprised of TaO_x ~~coupled to~~ and disposed over said bottom electrode;

~~a top electrode comprised of a layer of TiN and a layer of TaN coupled to said capacitor dielectric; and~~

~~sidewalls~~ dielectric sidewall structures comprised of SiN and disposed adjacent ~~to positioned at a perimeter of said top metal level capacitor; said sidewalls coupled to said top metal level,~~ said bottom electrode, and at least a portion of said capacitor dielectric~~, and a portion of said top electrode~~; and

~~wherein said layer of TaN of said~~ a top electrode comprising a first layer comprised of TiN disposed over and in contact with the capacitor dielectric, and a strap layer comprised of TiN that is disposed over the first layer and that extends over at least one dielectric sidewall structure to conductively contact ~~is coupled to~~ a second ~~interconnect~~ conductor of said top metal level~~, said first interconnect is coupled to a supply voltage and is comprised of copper, and said second interconnect is coupled to ground and is comprised of copper~~.

Claims 12 through 53 are canceled.

54 (new). The integrated circuit of Claim 1, wherein the top electrode comprises:

a first layer disposed over and adjacent to the capacitor dielectric; and

a conductive strap disposed over and in contact with the first layer, and extending over the at least one dielectric sidewall structure to the second conductor of the top metal level.

55 (new). The integrated circuit of Claim 54, wherein the conductive strap comprises a diffusion barrier material.

56 (new). The integrated circuit of Claim 54, wherein the dielectric sidewall structures are also disposed adjacent to at least a portion of the first layer of the top electrode.